

TPS56C215 4.5-V to 17-V Input (5-V External Bias), 12-A Synchronous Step-Down Converter

1 Features

- D-CAP3 Control Mode for Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.6 V to 5.5 V
- External 5-V Bias on VREG5 for Enhanced Efficiency Operation
- 0.6-V Vref with $\pm 1.5\%$ Accuracy Across Temperature
- Selectable Fsw of 400 kHz, 800 kHz and 1200 kHz
- Integrated 13.8 m Ω and 4.6 m Ω MOSFETs
- Selectable Forced Continuous Conduction Mode (FCCM) or Advanced Eco-mode™ Operation
- Three Adjustable Current Limit Settings with $\pm 15\%$ accuracy across temperature
- Adjustable Soft Start with a Default 1-ms Soft Start Time
- Open Drain PGOOD Output Indicator
- Monotonic Start Up into Pre-biased Outputs
- Cycle-by-Cycle Over-Current Limiting Control
- Hiccup Under-Voltage Protection
- Non-Latch OVP/UVLO/TSD Protections
- -40°C to 150°C Operating T_J Range
- Small 3.5-mm x 3.5-mm HotRod QFN Package

2 Applications

- Base Stations, Small Cells for Telecoms
- Cloud Server Application
- High-end DTV

3 Description

The TPS56C215 is a synchronous step down converter in a 3.5 mm x 3.5 mm Hotrod package that is designed to provide high efficiency till 14A with 13.5m Ω and 4.5m Ω integrated MOSFETs. It can operate from an input voltage of 4.5V to 17V. The device provides flexibility to the end user to target both high efficient and small footprint solutions by being able to choose between switching frequencies, current limit and mode settings.

The device employs D-CAP3 mode control that enables accurate output voltage and good transient response without the need of external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Advanced Eco-mode™ operation at light loads. The TPS56C215 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR, ceramic capacitors. There is an option to overdrive the internal LDO with an external 5V supply to boost the efficiency of the converter.

The under voltage lockout (UVLO) circuit monitors the VREG5 voltage to protect the internal circuitry from low input voltages. Hiccup current limit protection protects the device from short circuit conditions and the thermal shutdown disables the part when the die temperature exceeds thermal shutdown temperature.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS56C215	QFN (18)	3.5 mm x 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Output Current

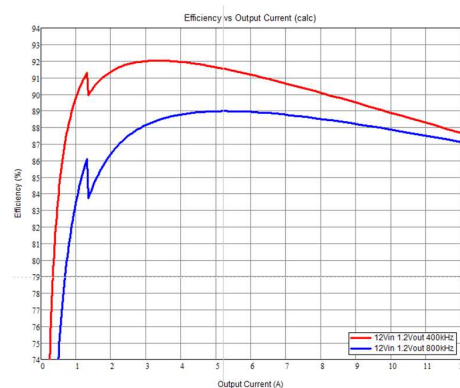


Table of Contents

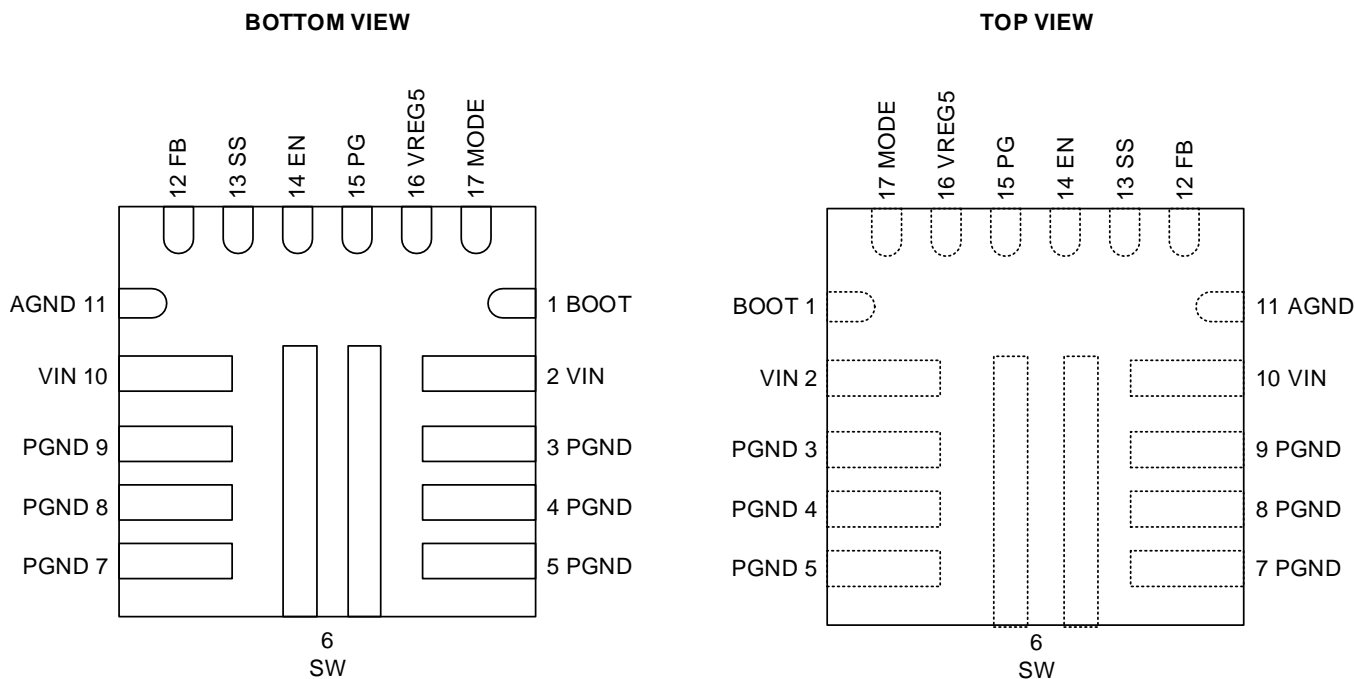
<p>1 Features 1</p> <p>2 Applications 1</p> <p>3 Description 1</p> <p>4 Revision History..... 2</p> <p>5 Pin Configuration and Functions 3</p> <p>6 Device and Documentation Support..... 4</p>	<p>6.1 Community Resources..... 4</p> <p>6.2 Trademarks 4</p> <p>6.3 Electrostatic Discharge Caution 4</p> <p>6.4 Glossary 4</p> <p>7 Mechanical, Packaging, and Orderable Information 4</p>
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4 Revision History

DATE	REVISION	NOTES
March 2016	*	Initial release.

5 Pin Configuration and Functions

RNN Package
17-Pin QFN with Thermal Pad



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect a 0.1uF ceramic capacitor between BOOT and SW.
VIN	2,11	P	Input voltage supply pin
PGND	3, 4, 5,8, 9, 10	G	GND terminal for the controller circuit and the internal circuitry
SW	6,7	O	Switch node
AGND	12	G	Ground of internal analog circuitry. Connect GND to PGND plane with a short trace.
FB	13	I	Converter feedback input. Connect to output voltage with resistor divider
SS	14	O	Connecting an external capacitor sets the SS time. If no external capacitor is connected the startup is with a default of 1 ms
EN	15	I	Enable input control, floats high.
PGOOD	16	O	Open Drain Power Good Indicator, becomes low if output voltage is low due to thermal shutdown, OV, EN shutdown or during SS.
VREG5	17	I/O	4.7-V LDO output that supplies internal circuitry and gate driver. Bypass it with a 2.2-μF capacitor
MODE	18	I	Connect this pin to a resistor divider between VREG5 and GND for different options

PRODUCT PREVIEW

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

Eco-mode, E2E are trademarks of Texas Instruments.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56C215RNNR	PREVIEW	VQFN	RNN	18	3000	TBD	Call TI	Call TI	-40 to 125		
TPS56C215RNNT	PREVIEW	VQFN	RNN	18	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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